Patent claims

1. A method to assemble a substrate (3; 21) for a semiconductor package (1, 18) comprising the following steps:
   - providing a substrate (3; 21) comprising a sheet of core material (5) and a plurality of upper contact traces (6) and upper contact pads (7) on its upper surface, a second plurality of lower conducting traces (8) and external contact areas (9) on its bottom surface and conducting vias (10) connecting the upper conducting traces (6) and lower conducting traces (8),
   - forming a plurality of vent holes (4) in the substrate (3), and
   - covering the upper and lower surfaces of the substrate (3; 21) by a layer of solder resist (15) leaving the contact areas (6 and 8) free from solder resist (15).

2. A method to assemble a substrate (21) according to claim 1 characterized in that
the vent holes (22) are closed at one end by a layer of solder resist (15) on the upper surface of the substrate (21).

3. A method to assemble a substrate (3) according to claim 1 or claim 2
characterized in that
the vent holes (4) are include solder resist (15).

4. A method to assemble a substrate (3; 21) according to one of claims 1 to 3
characterized in that
the vent holes (4, 22) are formed by drilling.

5. A method to assemble a substrate (3; 21) of one of claims 1 to 4
characterized in that
the vent holes (4) are formed in the core material (5) before a plurality of upper contact traces (6) and upper contact pads (7) on its upper surface, a second plurality of lower conducting traces (8) and external contact areas (9) on its bottom surface and conducting vias (10) are deposited.

6. A method to assemble a semiconductor package (1; 18; 20), comprising the following steps:
- providing the substrate (3; 21) with a method according to one of claims 1 to 5,
- providing a semiconductor chip (2) comprising an active surface including a plurality of chip contact areas (13),
- mounting the chip (2) on the upper surface of the redistribution board (3; 21) by microscopic solder balls (14) between the chip contacts (13) and upper contact areas (7),
- performing a solder reflow,
- underfilling the area between the chip (2) and the upper surface of the redistribution board (3; 21) with epoxy resin (16).

7. A method to assemble a semiconductor package (18)
characterized in that
the upper surface of the chip (2) and substrate (3; 21) are covered with mold material (19).

8. A substrate (3; 21) for a semiconductor package (1; 18; 20) comprising:
   - a sheet of core material (5),
   - a plurality of upper conducting traces (6) and upper contact pads (7) on its upper surface, a second plurality of lower conductive traces (8) and external contact areas (9) on its bottom surface and a plurality of conducting vias (10) connecting the upper conducting traces (6) and lower conducting traces (8),
   - a plurality of vent holes (4), and
   - a layer of solder resist (15) covering the upper and lower surfaces of the substrate (3) leaving the contact areas (6 and 8) free from solder resist (15).

9. A substrate (3) according to claim 8
characterized in that
the vent holes (4) are include solder resist (15).

10. A substrate (21) according to claim 8
characterized in that
the vent holes (22) are closed at one end by a layer of solder resist (15) on the upper surface of the substrate (21).

11. A substrate (3; 21) according to one of claims 8 to 10
characterized in that
the plurality of vent holes (4; 22) are laterally located towards the centre of the substrate (3; 21).

12. A substrate (3, 21) according to one of claims 8 to 11
characterized in that

the plurality of vent holes (4; 22) are laterally located towards the centre and towards the outer edges of the substrate (3, 21).

13. A substrate (3; 21) according to one of claims 8 to 12 characterized in that
the vent holes (4; 22) have a diameter of approximately 1µm to approximately 5mm or approximately 10µm to approximately 0.5mm or approximately 100µm.

14. A semiconductor package (1; 18; 20) comprising:
- a substrate (3; 21) according to one of claims 8 to 13,
- a semiconductor chip (2) including an active surface with a plurality of chip contact areas (13), electrically connected to the substrate (3; 21).

15. A semiconductor package (18; 20) according to claim 14 characterized in that
the chip (2) is encapsulated by mold material (19).

16. A semiconductor package (1; 18; 20) according to claim 14 or claim 15
characterized in that
the chip (2) is mounted to the substrate (3; 21) by the flip-chip technique.